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Addressing the Unbalance Loading Issue in Multi-Drive Systems with A DC-Link Modulation Scheme for Harmonic Reduction

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***Abstract*— Concerning cost, volume, and efficiency, Adjustable Speed Drive (ASD) systems are commonly employed with diode rectifiers or Silicon Controlled Rectifiers (SCR) as the front-ends (i.e., ac-dc converters). Apart from low cost, small volume, and high reliability, harmonic currents are significantly produced at the grid side by the rectification apparatus (i.e., diode rectifiers or SCR). As a simple strategy, the phase-shifted current control can be applied to the SCR-fed drive systems, where the input currents for the SCR are phase-shifted in such a way to cancel out the harmonics of interest (e.g., the 5th order harmonic). However, this solution is effective only when same amounts of currents are drawn by the rectifiers. Unfortunately, in practice, the loading is different among the parallel drive systems, leading to degradation in the harmonic mitigation. In this paper, unequal loading conditions in multi-drive systems are thus addressed. A load-adaptive scheme by means of varying the dc-link voltage is proposed, where a unified dc-link current modulation scheme is also employed in the dc-link. The proposed load-adaptive scheme can ensure that the rectified currents (i.e., rectifier output currents) are equal, and thus the harmonic reduction enabled by the phase-shifted current control is enhanced. The principle of the proposed method is demonstrated on a two-drive system consisting of a diode rectifier and a SCR. Experimental tests have validated the effectiveness of the proposed scheme in terms of harmonic mitigation for multiple parallel ASD systems.**

I. Introduction

Currently, around 65% of the industrial electrical energy is consumed by motors, which thus is calling for energy-efficient motor drives [1], [2]. Substantial energy savings are enabled by means of variable speed drive systems [3], [4], where Diode Rectifiers (DR) or Silicon-Controlled Rectifiers (SCR) employed as the front-ends (i.e., ac-dc converters) are still popular [5]–[7]. This is mainly due to low cost, simple control, small volume, and high reliability during operation in contrast to their counterparts, e.g., active front-end based drive systems [8]–[11] and multi-pulse transformer based drive units [11]–[16]. However, beyond the above benefits, either the DR- or the SCR-fed drive systems bring significant distorted currents to the grid that is connected to [6], [17]. If the harmonic issue is not properly addressed, the overall efficiency will be affected, violating the harmonic regulations or guidelines [18], [19] and potentially inducing resonance in the entire system.

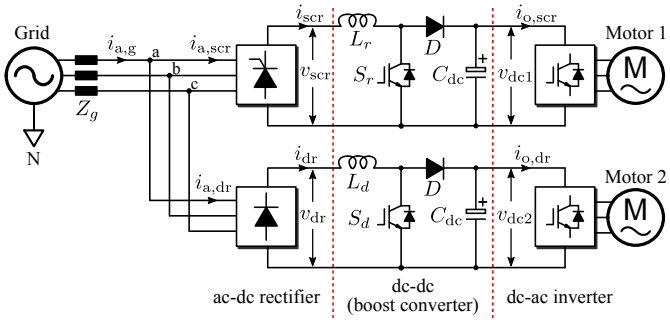

Fig. 1. Hardware schematic of a two-drive system consisting of a diode rectifier and a silicon-controlled rectifier, where dc-dc boost converters are adopted in the dc-links.

Typically, in the variable-frequency drive applications, the ac grid voltage is firstly rectified into a dc voltage, as it is exemplified in Fig. 1. It is observed that a dc-dc converter is adopted and placed into the dc-link in order to increase the control flexibility of the "uncontrolled" (DR) and the "half-controlled" (SCR) rectifiers, being a Power Factor Correction (PFC) circuit. This ac-dc configuration (i.e., ac-dc rectifier and dc-dc converter) offers one possibility to do proper modulations for the rectified currents (i.e., i_{scr} and i_{dr} in Fig. 1) in such a manner that the currents (e.g., $i_{a,scr}$ and $i_{a,dr}$ in Fig. 1) drawn from the grid by the rectifiers can be "modulated" (controlled), as it has been discussed in [2], [20] and [21]. At the same time, owing to the PFC system, it is also possible to control the dc-link voltage (i.e., $v_{dc1,2}$ in Fig. 1) to be constant (e.g., 700 V), which is independent of the actual grid voltage [5]. Nevertheless, with the PFC configuration demonstrated in Fig. 1, the total grid currents (e.g., $i_{a,g}$ in Fig. 1) can be modulated as multi-level, where certain targeted harmonics (e.g., the 5th order harmonic) can be mitigated in theory. This will contribute to improved quality of the grid currents in terms of a lower Total Harmonic Distortion (THD), which is demanded in relevant standards [18].

In addition, in the case of multi-drive systems consisting of parallel SCR-fed drives, by shifting the SCR currents,

the total grid current quality can be further enhanced [17], being a phase-shifted current control [21]. Taking the two-drive system shown in Fig. 1 as an example, in particular, when the rectified currents (e.g., $i_{\rm scr}$ and $i_{\rm dr}$ in Fig. 1) are controlled as dc currents at the same level through dc-dc converters (e.g., a boost converter), the total grid current becomes multi-level. As a consequence, an even better THD of the grid currents is achieved. However, the effectiveness of this harmonic mitigation strategy is affected by the loading conditions of the parallel drive systems. That is to say, if the currents drawn by multiple parallel drive units are not equal, the harmonic cancellation enabled by the phase-shifted current control cannot be accomplished completely [21]. Moreover, in practice, all the drive units are rarely operating at the same loading condition. As a result, the harmonic mitigation enabled by the phase-shifted current control even with the dc-link modulation scheme will be degraded.

In order to address the above issues, this paper proposes a load-adaptive phase-shifted control scheme, which can ensure that each drive unit draws the same amount of currents from the grid. The principle of the load-adaptive scheme is demonstrated on a two-drive system referring to Fig. 1. Firstly, a unified dc-link modulation scheme aiming at selective harmonic cancellations is introduced in § II, followed by the load-adaptive scheme. Experimental tests have been conducted, and the results are presented in § IV, which validate the effectiveness of the load adaptive phase-shifted current control in terms of harmonic cancellations in multi-drive systems. Finally, § V draws the conclusions.

II. Unified DC-Link Modulation Scheme

As mentioned, for the drive system with a dc-dc converter in the dc-link, it is possible to apply advanced modulation schemes, which makes the system behave as a PFC system [5]. In that case, the dc-link voltage can also be adjusted to a constant level (e.g., 700 V). In order to implement the dc-link current modulation scheme, a desired current pattern should be designed and pre-programmed, as it is illustrated in Fig. 2, where it shows how the unified dc-link current modulation scheme is synthesized. Specifically, referring to Fig. 1, when assuming that the grid voltages (e.g., the line-line voltages $v_{\rm ab}$, $v_{\rm bc}$, and $v_{\rm ca}$) are balance, the rectified output voltage (i.e., $v_{\rm scr}$ and $v_{\rm dr}$ in Fig. 1) will contain six identical segments with a conduction angle of 60° for each [22], [23]. As a consequence, it is feasible to synthesize the reference for the rectified output current (i.e., $i_{\rm scr}$ and $i_{\rm dr}$ in Fig. 1) by summing up the absolute three-phase desired current signals, as it is highlighted in Fig. 2. This is the principle of the unified current modulation scheme for the dc-link with a dc-dc converter. As long as a specific desired current signal is designed and implemented according to Fig. 2, the phase currents drawn by the rectifiers (e.g., $i_{\rm a,scr}$ and $i_{\rm a,dr}$ in Fig. 1) will follow the shape of the designed current signal. It explains the possibility to cancel out certain harmonics by designing a proper desired current signal. The following gives two modulation signals, which makes the grid currents "three-level" and "five-level", respectively.

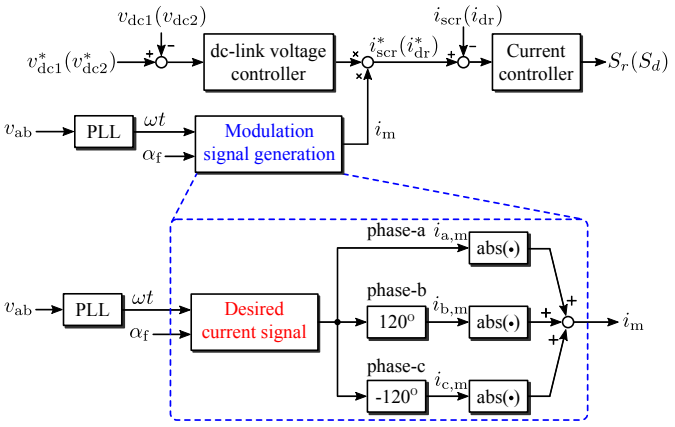

Fig. 2. Control block diagrams of the dc-dc boost converter as the dc-link in a SCR-fed or a DR-fed drive system (Fig. 1) with the unified dc-link current modulation scheme (PLL - Phase Locked Loop), where $v_{\rm ab}$ is the grid line-line voltage and $\alpha_{\rm f}$ is the SCR firing angle (in the case of a DR-fed drive system, $\alpha_{\rm f}$ = 0).

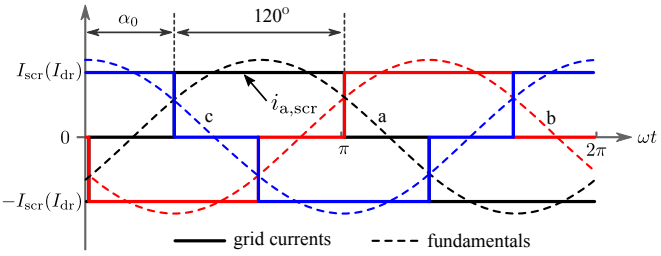

Fig. 3. Typical mains current waveforms of a SCR-fed or a DR-fed drive system when the rectified currents are controlled as purely dc, in which $\alpha_0 = \pi/6 + \alpha_{\rm f}$ (in the case of a DR-fed drive system, $\alpha_{\rm f}$ = 0).

A. Square Modulation Signal

For the rectifiers shown in Fig. 1, if the rectified currents (e.g., $i_{\rm scr}$ and $i_{\rm dr}$) are controlled as purely dc currents (denoted as $I_{\rm scr}$ and $I_{\rm dr}$, respectively), the mains current will be of a square waveform [21], [22], as it is shown in Fig. 3. Hence, a simple modulation signal can be generated by taking the rectangular waveform of phase-a shown in Fig. 3 as the desired current signal that should be implemented according to Fig. 2. By doing so, the grid currents will be rectangular waveforms (see Fig. 3), but it brings significant distortions to the grid, which is further illustrated by means of a Fourier analysis.

According to Fig. 3, applying the Fourier analysis to a specific phase current of the SCR unit (e.g., $i_{\rm a,scr}$) yields

$$i_{\rm a,scr}(t) = \sum_{h}^{\infty} i^h_{\rm a,scr}(t) = \sum_{h}^{\infty} \left[a^h \cos(h\omega t) + b^h \sin(h\omega t)\right] \tag{1}$$

in which $i^h_{\rm a,scr}(t)$ is the $h^{\rm th}$ order harmonic of the grid current $i_{\rm a,scr}(t)$ drawn by the SCR, and a^h, b^h are the Fourier coefficients that can be calculated by

$$\begin{cases} a^h = \dfrac{2}{\pi}\displaystyle\int_0^{\pi} i_{\rm a,scr}(t)\cos(h\omega t)\,d(\omega t) \\ b^h = \dfrac{2}{\pi}\displaystyle\int_0^{\pi} i_{\rm a,scr}(t)\sin(h\omega t)\,d(\omega t) \end{cases} \tag{2}$$

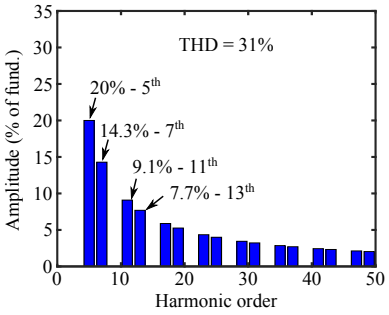

Fig. 4. Harmonic distributions of the rectangular grid currents shown in Fig. 3 when the dc-link modulation scheme is implemented according to Fig. 2.

with h = 1, 3, 5, ... being the harmonic order and ω being the angular grid frequency. Subsequently, the Root-Mean-Square (RMS) value of the h^{th} order harmonic in the grid current can be obtained as

$$I^h_{\text{a, scr}} = \frac{\sqrt{2}}{2}\left[(a^h)^2 + (b^h)^2\right]^{1/2} \tag{3}$$

where $I^h_{\text{a, scr}}$ is the RMS magnitude of the h^{th} harmonic current.

Accordingly, the harmonic distributions of the resultant rectangular grid currents discussed above can be obtained as demonstrated in Fig. 4. It can be observed in Fig. 4 that the square modulation signal implemented according to the unified dc-link current modulation scheme (see Fig. 2) will contribute to a poor current quality with the THD of 31%, although the grid currents become three-level. In particular, the low-order harmonics (e.g., the 5th, the 7th, the 11th, and the 13th) are significant, which however are not desired in the ASD applications. Hence, advanced schemes to mitigate these harmonics should be developed in order to achieve a satisfied power quality.

B. Five-Level Modulation Signal

In order to cancel out certain harmonics of the square waveforms in Fig. 3, a five-level modulation signal has been designed for the unified dc-link modulation scheme. Fig. 5 shows the generation process of the desired five-level modulation signal for phase-a in a SCR system, i.e., $i_{\text{a,m}}$. It can be identified in Fig. 5 that the five-level desired current signal is composed of three rectangular waveforms (i.e., $i_{\text{a,m}} = i_{\text{rw1}} + i_{\text{rw2}} - i_{\text{rw3}}$). Furthermore, it is shown that these square signals (i.e., #1 – i_{rw1}, #2 – i_{rw2}, and #3 – i_{rw3}) have a conduction angle of β_1 (120°), β_2, and β_3, a phase-shift of α_1, α_2, and α_3, and an amplitude of I^1_{dc}, I^2_{dc}, and I^3_{dc}, correspondingly. Additionally, for the DR-fed dc-dc converter, a five-level modulation signal can also be generated by setting α_{f} = 0. That is to say, all the waveforms shown in Fig. 5 will be shifted back by a degree of α_{f} (i.e., α_1 = 30°). It should be noted further that, in order to avoid triplen harmonics, the square signals (i_{rw2} and i_{rw3}) should be centered in respect to the square signal #1 – i_{rw1}, as annotated in Fig. 5. Moreover, the levels (i.e., $I^1_{\text{dc}} + I^2_{\text{dc}}$) of the desired signal should be symmetrical, and thus

$$\beta_1 = \beta_2 + \beta_3 = 120^\circ \tag{4}$$

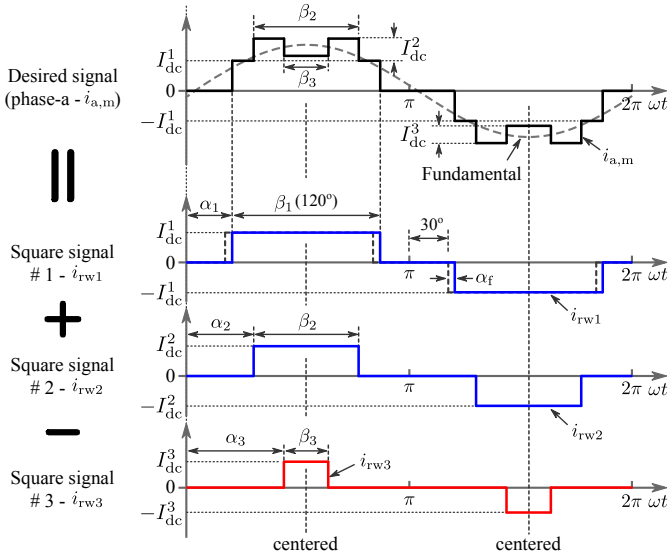

Fig. 5. Generation of a five-level modulation signal (phase-a) for the unified dc-link modulation scheme with the purpose of canceling out certain low-order harmonics using three rectangular signals (i.e., i_{rw1}, i_{rw2}, and i_{rw3}).

which should be considered during the design phase as well as optimization of the five-level modulation signal.

According to Fig. 5, the h^{th} order harmonic component of each rectangular waveform used to generate the five-level modulation signal can be identified as

$$i^h_{\text{rw}k}(t) = a^h_k \cos(h\omega t) + b^h_k \sin(h\omega t) \tag{5}$$

with k = 1, 2, 3 being the signal index, a^h_k and b^h_k being the corresponding Fourier coefficients. Substituting the k-th square signal (i.e., $i_{\text{rw}k}(t)$) into (2) to replace $i_{\text{a,scr}}(t)$ gives the Fourier coefficients as

$$\begin{cases} a^h_k = \dfrac{2I^k_{\text{dc}}}{h\pi}\left[-\sin(h\alpha_k) + \sin(h\alpha_k + h\beta_k)\right] \\ b^h_k = \dfrac{2I^k_{\text{dc}}}{h\pi}\left[\cos(h\alpha_k) - \cos(h\alpha_k + h\beta_k)\right] \end{cases} \tag{6}$$

where h is the harmonic order as defined previously.

As aforementioned, when the five-level modulation signal is implemented according to Fig. 2, the currents drawn from the grid (i.e., $i_{\text{a,scr}}$) will follow the desired five-level current signal. According to the superposition principle, Fig. 5, and (5), the harmonic component of the resultant grid phase-a current (i.e., $i_{\text{a,scr}}(t)$) will follow

$$i^h_{\text{a,m}}(t) = (a^h_0 + a^h_1 - a^h_2)\cos(h\omega t) + (b^h_0 + b^h_1 - b^h_2)\sin(h\omega t) \tag{7}$$

and its RMS magnitude can then be obtained as

$$I^h_{\text{a,m}} = \frac{\sqrt{2}}{2}\left[\left(a^h_0 + a^h_1 - a^h_2\right)^2 + \left(b^h_0 + b^h_1 - b^h_2\right)^2\right]^{1/2} \tag{8}$$

As a consequence, in order to eliminate certain harmonics with the desired five-level modulation scheme, the corresponding harmonic amplitude should be zero. Specifically, if $I^h_{\text{a,m}}$ = 0 with $h \neq 1$ is solved, the h^{th} order harmonic will be completely canceled in theory.

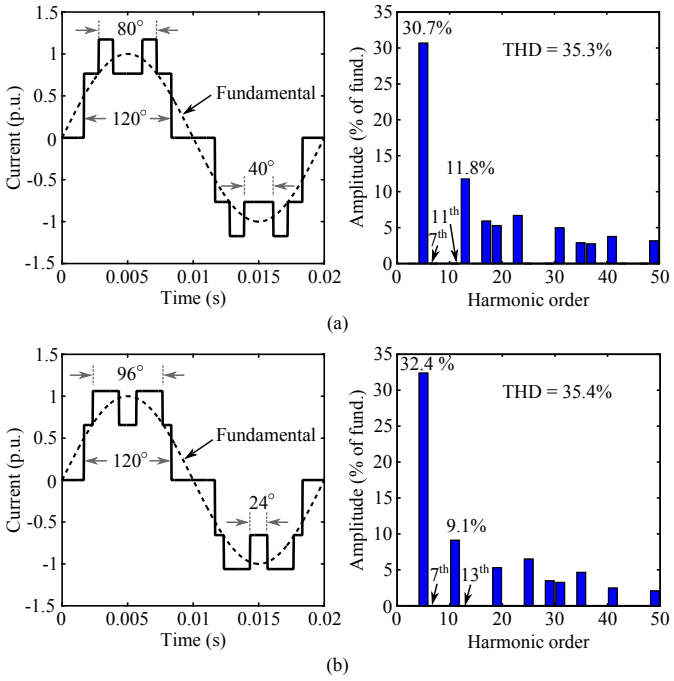

Fig. 6. Examples of five-level modulation signals that can be implemented into the unified dc-link current modulation scheme for selectively mitigating: (a) the 7th and the 11th harmonics with $I_{\rm dc}^1$ = 0.765 p.u., $I_{\rm dc}^2 = I_{\rm dc}^3$ = 0.408 p.u., β_2 = 80° and (b) the 7th and the 13th harmonics with $I_{\rm dc}^1$ = 0.656 p.u., $I_{\rm dc}^2 = I_{\rm dc}^3$ = 0.406 p.u., β_2 = 96°, where $\alpha_{\rm f}$ = 0.

Fig. 6 demonstrates two examples of the five-level modulation signal designed according to Fig. 5, where a Global Search Algorithm [24] has been adopted to solve the equations (i.e., (4) through (8)), noted that other software (e.g., the EES - Engineering Equation Solver from F-Chart Software, LLC) is also applicable. It can be observed in Fig. 6 that, with a five-level modulation signal, selective harmonic cancellations are enabled, when it is implemented according to the unified dc-link modulation scheme shown in Fig. 2. However, due to the inherent relationships among the harmonics, it is impossible to cancel out the 5th and the 7th harmonics at the same time. Moreover, also because of this cross-impact, when certain harmonics are completely mitigated (e.g., the 7th and the 11th), some of the rest harmonics within the spectrum will be exaggerated in contrast to those shown in Fig. 4, leading to a high THD of the resultant currents. In order to improve the current quality, a phase-shifted current control scheme is introduced in the following, where the unequal loading impact is also taken into account.

III. Load-Adaptive Phase-Shifted Current Control Scheme

A. Principle of Phase-Shifted Control

The above has demonstrated the unified dc-link current modulation scheme for three-phase rectifiers, which enables the flexibility to control the currents drawn from the grid. However, in order to ensure the performance (i.e., the rectified currents follow the desired modulation signals as exemplified in Fig. 5), the current controllers as shown in Fig. 2 should be taken care of. In particular, the current dynamics have to be fast enough in such a way that the grid currents will be as close to the designed modulation signal as possible. In light of this, hysteresis controllers have been employed, and thus guaranteeing the control effectiveness of the grid currents.

Additionally, as exemplified in Figs. 4 and 6, the unified dc-link current modulation scheme can only achieve a selective harmonic mitigation in a cost- and size-effective way, rather than an improved current quality. In practice, multiple ASD systems may operate in parallel, and be connected to the point of common coupling (e.g., Fig. 1). This initiates the phase-shifted current control to further improve the current quality, where SCR-fed drives should be utilized. To illustrate, the two-drive system is taken as an example. According to Fig. 3 and (1), the corresponding $h^{\rm th}$ harmonic components of the SCR and the DR can be represented as phasors,

$$\mathbf{I}_{\rm a,scr}^h = \sqrt{2} I_{\rm a,scr}^h e^{j\phi_{\rm a,scr}^h} \text{ and } \mathbf{I}_{\rm a,dr}^h = \sqrt{2} I_{\rm a,dr}^h e^{j\phi_{\rm dr}^h} \tag{9}$$

with $I_{\rm a,scr}^h$ and $I_{\rm a,dr}^h$ being the RMS magnitudes, $\phi_{\rm a,scr}^h$ and $\phi_{\rm a,dr}^h$ being the phases of the $h^{\rm th}$ order harmonic of the SCR and the DR, respectively. The magnitudes and the phases of an individual harmonic can be calculated using the corresponding Fourier coefficients [22].

According to the superposition principle and (9), the phasor of the $h^{\rm th}$ order harmonic component appearing in the grid (i.e., $i_{\rm a,g}$ in Fig. 1) can be obtained as

$$\mathbf{I}_{\rm a,g}^h = \mathbf{I}_{\rm a,scr}^h + \mathbf{I}_{\rm a,dr}^h = \sqrt{2} I_{\rm a,scr}^h e^{j\phi_{\rm a,scr}^h} + \sqrt{2} I_{\rm a,dr}^h e^{j\phi_{\rm a,dr}^h} \tag{10}$$

which indicates that the $h^{\rm th}$ order grid current harmonic can be fully mitigated, only when

$$I_{\rm a,scr}^h = I_{\rm a,dr}^h \text{ and } \phi_{\rm a,scr}^h = \phi_{\rm a,dr}^h - \pi \tag{11}$$

where the latter criterion can be fulfilled by properly introducing a phase shift to the SCR of Fig. 1 (i.e., $\alpha_{\rm f} = 180°/h$). However, in practice, the magnitudes of the currents drawn by the rectifiers (or the rectified current amplitudes) cannot be always the same (i.e., $I_{\rm a,scr}^h \neq I_{\rm a,dr}^h$), as discussed previously and elaborated in Fig. 7. It is demonstrated in Fig. 7 that incomplete cancellation of the 5th order harmonic by introducing a phase shift of 180°/5 (i.e., $\alpha_{\rm f}$ = 36°) occurs, when the magnitudes of the currents are not equal. As a consequence of the unbalanced loading condition, the performance of the phase-shifted current control is degraded, and the 5th order harmonic appears again in the grid current. Thus, load-adaptive schemes should be developed to ensure that conditions in (11) are always satisfied during operation.

Nevertheless, the phase-shifted current control combined with the five-level modulation schemes (see Fig. 6) can significantly enhance the grid current quality. Fig. 8 gives an example of the resultant grid current, assuming that the two drives are drawing the same amount of currents from the grid. As exemplified, the grid current become even multi-level, and a low THD of 12% is reached. Furthermore, since the firing angle for the SCR has been set as $\alpha_{\rm f}$ = 36°, the 5th order and

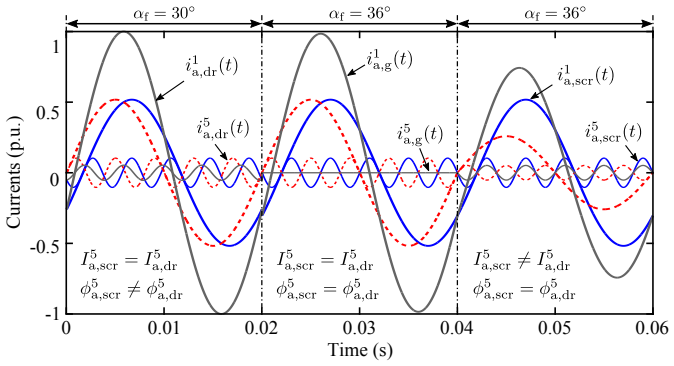

Fig. 7. Illustration of the unbalanced loading impact on the performance of phase-shifted current control in harmonic cancellations, where only the fundamental (denoted by the subscript - 1) currents and the 5th order (denoted by the subscript - 5) harmonic currents are shown.

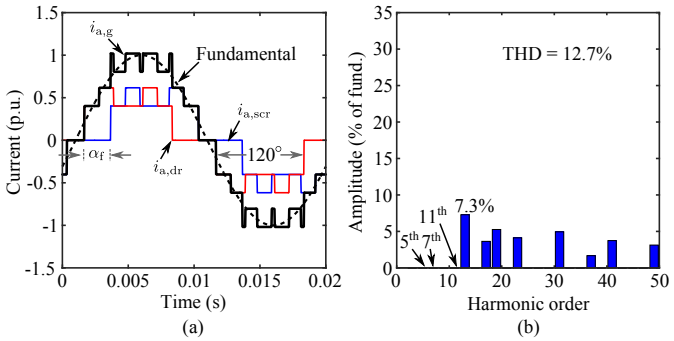

Fig. 8. Grid current harmonic characteristics of the two-drive system with the phase-shifted current control (α_f = 36°), where the five-level modulation signal (Fig. 6(a)) has been applied to both rectifiers according to the unified dc-link modulation scheme: (a) grid current waveform and (b) harmonic distributions of the grid current.

the harmonics of fivefold the grid fundamental frequency are all eliminated by the phase-shifted control, in contrast to these harmonic contents shown in Fig. 6(a).

B. Load-Adaptive Control Scheme

As it is shown in Fig. 7, unequal loading will result in an incomplete cancellation of the harmonics of interest (e.g., the 5th order harmonic). Hence, a load-adaptive control scheme is proposed in the following. It is clear to all that the firing angle α_f controls the SCR input current phase (e.g., the phase-a current drawn from the grid as $i_{a,scr}$ in Fig. 1), and also the average rectified voltage that is given as

$$\bar{v}_{scr} = \bar{v}_{dr} \cos \alpha_f = \frac{3}{\pi} V_{LL} \cos \alpha_f \tag{12}$$

where $\bar{v}_{scr}$, $\bar{v}_{dr}$ are the average rectified voltages of the SCR and the DR, respectively, and V_{LL} is the amplitude of the line-to-line voltages (e.g., v_{ab}) of a balanced grid. On the condition that communication is available in the multi-drive system shown in Fig. 1, the loading information can then be obtained, where a power ratio γ and a load current ratio λ are defined as

$$\gamma = \frac{P_{scr}}{P_{dr}} \text{ and } \lambda = \frac{\bar{i}_{o,scr}}{\bar{i}_{o,dr}} \tag{13}$$

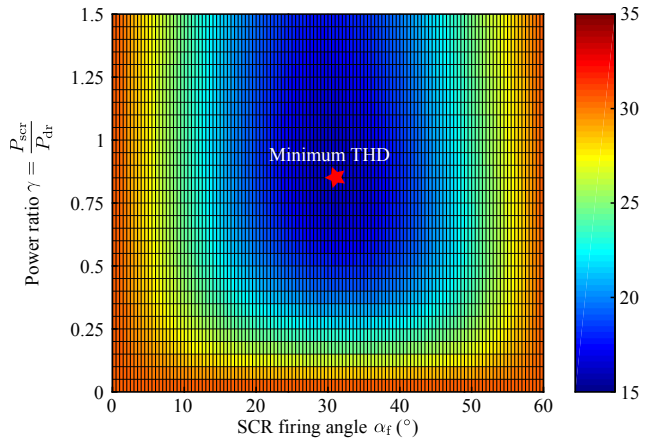

Fig. 9. THD distribution of the grid currents (e.g., phase-a $i_{a,g}$) in the two-drive system with the phase-shifted control (different firing angles for the SCR), where the square modulation signal (see § II.A) has been employed for both rectifiers.

with $P_{scr} = \bar{v}_{dc1} \cdot \bar{i}_{o,scr}$ and $P_{dr} = \bar{v}_{dc2} \cdot \bar{i}_{o,dr}$ being the boost output powers (i.e., the input powers for the inverters), where $\bar{i}_{o,scr}$ and $\bar{i}_{o,dr}$ are the average load currents, and $\bar{v}_{dc1}$ and $\bar{v}_{dc2}$ are the average dc-link voltages, respectively.

Ignoring the power losses on the boost converters gives $P_{scr} \approx \bar{v}_{scr} \cdot I_{scr}$ and $P_{dr} \approx \bar{v}_{dr} \cdot I_{dr}$. Thus, the following can be obtained:

$$\gamma = \frac{P_{scr}}{P_{dr}} = \frac{\bar{v}_{dc1} \cdot \bar{i}_{o,scr}}{\bar{v}_{dc2} \cdot \bar{i}_{o,dr}} \approx \frac{\bar{v}_{scr} \cdot I_{scr}}{\bar{v}_{dr} \cdot I_{dr}} \tag{14}$$

where I_{scr} and I_{dr} are averages of the rectified currents (controlled as dc) of the SCR and the DR, respectively. Substituting (12) into (14) yields

$$\gamma = \frac{P_{scr}}{P_{dr}} \approx \frac{I_{scr}}{I_{dr}} \cos \alpha_f \tag{15}$$

Then, with the knowledge of the loading information, it is possible to obtain the resultant grid current quality of the two-drive system (see Fig. 1), as shown in Fig. 9, where the square modulation signal discussed in § II.A has been adopted for the two rectifiers. It is further demonstrated that, under unbalanced loading between the two rectifier-fed drives, the grid current quality is affected. This impact is related to the power ratio (unbalance condition) as well as the phase shift angle. More important, it can be observed in Fig. 9 that a minimum THD of 16% (red star) is achieved at around γ = 0.848 and α_f = 32°, corresponding to $I_{scr} = I_{dr}$.

Consequently, in order to ensure the performance of the phase-shifted current control, the load-adaptive control scheme should always maintain $I_{scr} = I_{dr}$, which accordingly results in $\gamma = \cos \alpha_f$. To accomplish this, the dc-link reference voltages for the two rectifier systems should be set in accordance to

$$\frac{v^*_{dc1}}{v^*_{dc2}} = \frac{\cos \alpha_f}{\lambda} \tag{16}$$

where v^*_{dc1} and v^*_{dc2} are the dc-link reference voltages for the SCR and the DR rectifier system, respectively. It should be noted that in order to ensure proper operation of the boost

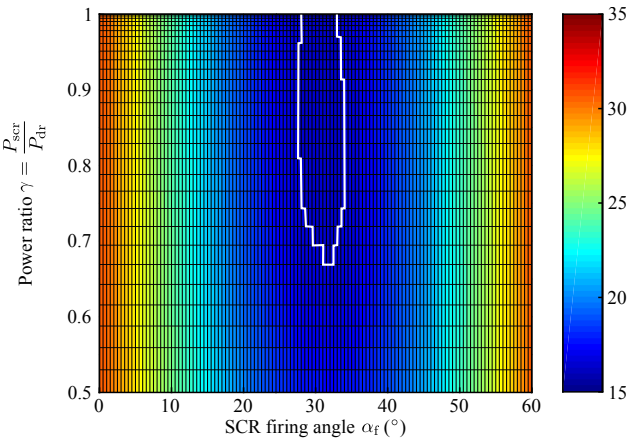

Fig. 10. THD distribution of the grid currents (e.g., phase-a $i_{a,g}$) in the two-drive system with the load-adaptive phase-shifted control and the square modulation signal, when the SCR is operating at partial loading condition.

converters, $v^*_{dc1} \geq v_{scr}$ and $v^*_{dc2} \geq v_{dr}$. If (16) is included in the control scheme shown in Fig. 2, the amounts of currents drawn by both rectifier systems will be equal, leading to an effective harmonic cancellation enabled by the phase-shifted current control. In that case, the SCR should operate in partial loading, i.e., $P_{scr} = P_{dr} \cos \alpha_f$, as shown in Fig. 10. It is highlighted in Fig. 10 that the SCR should be operated with 75% to 100% loading of the DR system and the firing angle of 28° to 34° (i.e., the white line zone), where the THD of the grid current will be 16% to 18%. Additionally, when the voltage references are set according to (16), the unified dc-link modulation scheme associated with the phase-shifted current control becomes load-adaptive no matter what modulation signals are used, and thus benefiting for harmonic reduction in multi-drive applications.

IV. Experimental Results

In order to verify the discussion, experiments have been carried out on a two-drive system, referring to Figs. 1 and 2. The system parameters are given in Table I. The control algorithms are implemented in digital signal processors. A hysteresis controller is adopted to control the rectified currents (i.e., i_{scr} and i_{dr}). The output dc-link voltages (i.e., v_{dc1} and v_{dc2}) are controlled through a Proportional Integral (PI) controller for each drive, and the PI transfer function in the z-domain is given as

$$G_{PI}(z) = k_p + \frac{k_i T_s}{2} \cdot \frac{1 + z^{-1}}{1 - z^{-1}} \tag{17}$$

with k_p and k_i are the gains of the PI controller, and T_s is the sampling period. All the control parameters are listed in Table I. It should be noted that in the experimental tests resistive loads have been used. A second order generalized integrator based PLL system has been employed to synchronize, and its design can be found in [25].

Two cases are studied to validate the unequal loading impact on the harmonic cancellation. In the first case, the load resistors are the same for both rectifiers, and the experimental

TABLE I
Parameters of the Multi-Drive System (Fig. 1).

Parameter	Symbol	Value
DC-link inductor	L_r, L_d	2 mH
DC-link capacitor	C_{dc}	470 μF
SCR output voltage reference	v^*_{dc1}	650 V
Grid frequency	f_g	50 Hz
Grid phase voltage (RMS)	$v_{abc,\,N}$	220 V
Grid impedance	Z_g (L_g, R_g)	0.18 mH, 0.1 Ω
PI controller	k_p, k_i	0.01, 0.1
Hysteresis band	-	2 A

results are shown in Fig. 11, where the square modulation signal has been implemented according to the unified dc-link modulation scheme (see Fig. 2) and α_f = 32°, v^*_{dc2} = v^*_{dc1} = 650 V. It can be seen in Fig. 11(a) that, with the phase-shifted current control, the THD of the grid current in the two-drive system has been brought to 16.3%, which is close to the theoretical value (16% in Fig. 9). The difference is induced by the unequal currents that are drawn by the rectifiers (i.e., $I_{scr} \neq I_{dr}$), although the output powers are almost the same. Subsequently, the load-adaptive scheme is applied to the drive system, where the dc-link output voltage for the DR has been changed to v^*_{dc2} = 705 V. As it is shown in Fig. 11(b), the grid current THD is lowered to 16% as the theoretical one. Furthermore, it is observed that, by changing the dc-link voltage reference, the load-adaptive phase-shifted current scheme can ensure the input currents of both rectifiers are at the same level, and the SCR is operating at partial loading condition in respect to the power of the DR (i.e., $P_{scr} \approx P_{dr} \cos \alpha_f$).

In the second study case, the loading of the SCR is around 80% of the DR (i.e., $\lambda \approx 0.8$ and $\bar{i}_{o,scr} \approx 0.8\bar{i}_{o,dr}$), if the dc-link voltage references are the same (i.e., v^*_{dc1} = v^*_{dc2}). This will lead to unequal input currents for the rectifiers, and thus it will deteriorate the phase-shifted current control in terms of higher THD of the grid currents. Hence, in order to enhance the harmonic cancellation performance, the dc-link voltage reference for the DR-fed boost converter is reduced to v^*_{dc2} = 630 V according to (16) with α_f = 32°. As it is shown in Fig. 12, the load-adaptive phase-shifted current control can maintain an almost-equal-current drawing from the grid for the rectifiers, and thus the grid current quality is enhanced. The slight current difference (i.e., $I_{scr} \approx I_{dr}$ in Fig. 12) is induced by the resistance variations in the resistive loads (e.g., temperature rises during operation). Nevertheless, the above cases have demonstrated the effectiveness of the load-adaptive phase-shifted current control scheme in multi-drive applications, where thus the unbalanced loading issues are addressed.

In addition to the above cases with the square modulation signal, more tests have been carried out on the same setup, where the five-level modulation signal shown in Fig. 6(a) has

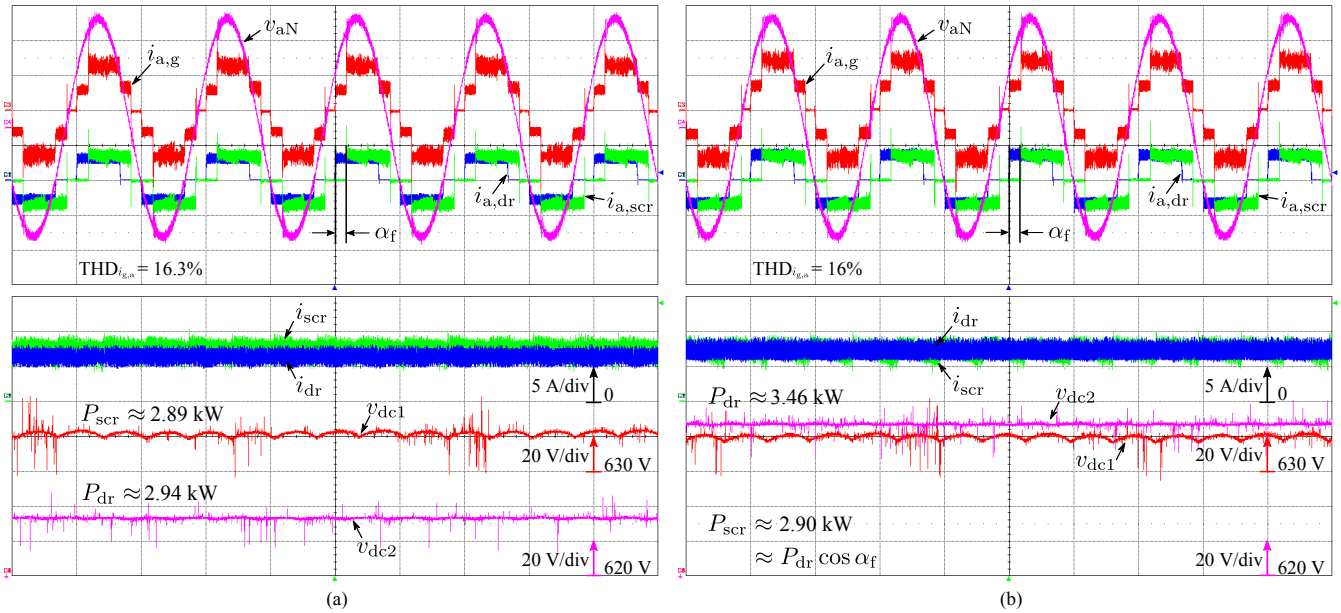

Fig. 11. Experimental results of the two-drive system with the unified dc-link current modulation scheme (square modulation signal), where the phase-shift for the SCR is $\alpha_f = 32°$ (top: grid voltage v_{aN} [100 V/div], grid current $i_{a,g}$ [10 A/div], SCR input current $i_{a,scr}$ [10 A/div], DR input current $i_{a,dr}$ [10 A/div], time [10 ms/div]; bottom: SCR rectified current i_{scr}, DR rectified current i_{dr}, SCR dc-link voltage v_{dc1}, DR dc-link voltage v_{dc2}, time [5 ms/div]): (a) without the load-adaptive scheme (power factor: 0.94) and (b) with the load-adaptive control scheme (power factor: 0.94).

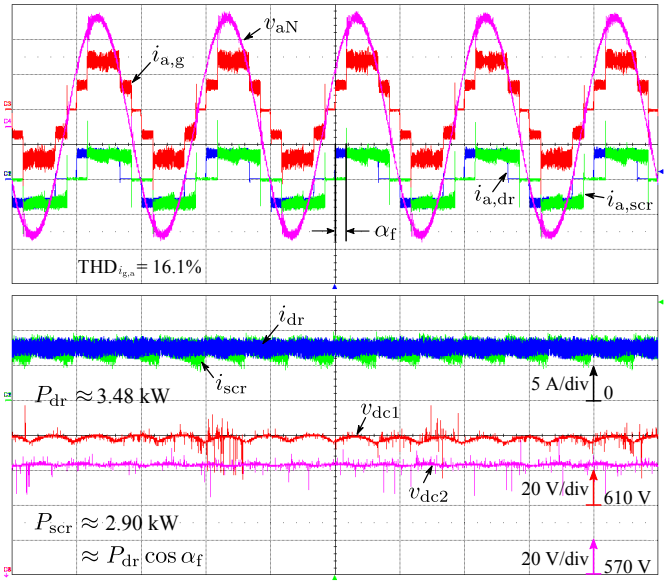

Fig. 12. Experimental results of the two-drive system with the unified dc-link current modulation scheme (square modulation signal) and the load-adaptive control scheme, where $\alpha_f = 32°$ and the power factor is 0.94. (top: grid voltage v_{aN} [100 V/div], grid current $i_{a,g}$ [10 A/div], SCR input current $i_{a,scr}$ [10 A/div], DR input current $i_{a,dr}$ [10 A/div], time [10 ms/div]; bottom: SCR rectified current i_{scr}, DR rectified current i_{dr}, SCR dc-link voltage v_{dc1}, DR dc-link voltage v_{dc2}, time [5 ms/div]).

been implemented into both rectifier systems. In this case study, the resistors are the same, and a phase-shift of 36° has been introduced to the SCR in order to mitigate the harmonics of fivefold the fundamental grid frequency. According to the discussions in § III and the previous experimental tests, the dc-link voltage references should be set considering the constraints of (16), in such a way that the averages of the rectified currents will be equal, leading to improved grid current quality. Thus, v^*_{dc1} = 650 V, while v^*_{dc2} = 720 V. The experimental results are presented in Fig. 13.

It can be seen from Fig. 13 that, with the unified dc-link current modulation scheme, the currents drawn by the rectifiers can be flexibly shaped or controlled (e.g., as the five-level waveforms shown in Fig. 6(a)). As a consequence of the load-adaptive phase-shifted current control, the resultant grid current becomes even multi-level, similar to the shape of Fig. 8(a). Hence, the grid current THD can be lowered to 11.6%, as shown in Fig. 13. Additionally, in contrast to the theoretical harmonic distribution shown in Fig. 8(b), the low-order harmonics (i.e., the 5th, the 7th, and the 11th) are not completely eliminated, but are also relatively low with the unified dc-link modulation scheme. In all, the experimental tests have demonstrated that the load-adaptive phase-shifted control employed with the unified dc-link current modulation scheme can contribute to significant improvements of the grid current quality in motor drive applications. This lies in: 1) the flexibility to design the desired modulation signals for selective harmonic mitigation and 2) the enhancement of harmonic cancellation enabled by the load-adaptive phase-shifted current control scheme.

V. Conclusion

In this paper, the unequal loading condition induced harmonic mitigation degradation of a phase-shifted current control scheme has been addressed in the DR and the SCR based three-phase motor drive applications, where dc-dc boost

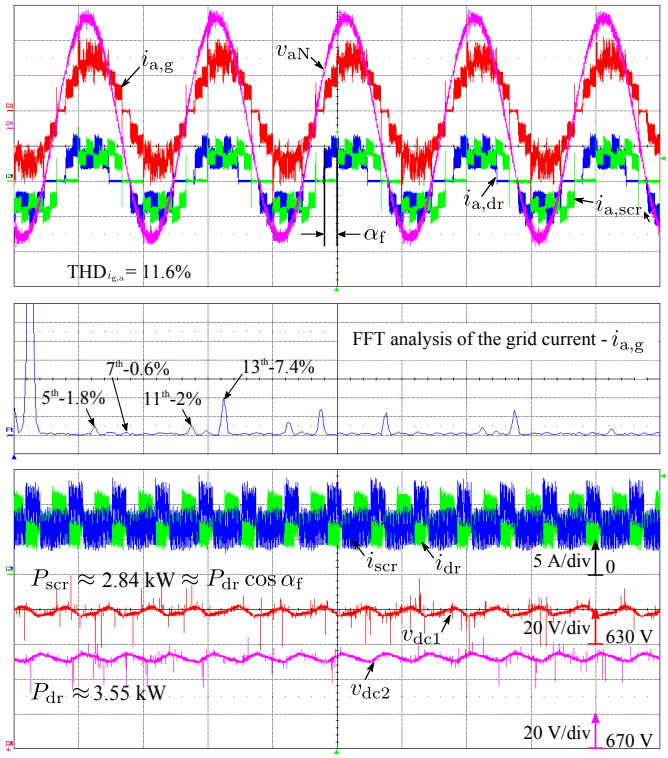

Fig. 13. Experimental results of the two-drive system with the unified dc-link current modulation scheme (five-level modulation signal shown in Fig. 6(a)) and the load-adaptive control scheme, where $\alpha_f = 36^\circ$ and the power factor is 0.93. (top: grid voltage v_{aN} [100 V/div], grid current $i_{a,g}$ [10 A/div], SCR input current $i_{a,scr}$ [10 A/div], DR input current $i_{a,dr}$ [10 A/div], time [10 ms/div]; middle: Fast Fourier Transform - FFT of the grid phase-a current [500 mA/div], frequency [200 Hz/div]; bottom: SCR rectified current i_{scr}, DR rectified current i_{dr}, SCR dc-link voltage v_{dc1}, DR dc-link voltage v_{dc2}, time [5 ms/div]).

converters are employed in the dc-link. A unified dc-link current modulation scheme is also applied to the rectifiers in such a way to shape the currents drawn from the grid, and thus to further mitigate the harmonics of interest. Together with the phase-shifted current control, the grid current quality can be improved a lot. However, the performance of this harmonic mitigation strategy (i.e., the phase-shifted current control) is affected by the loading among the paralleled drive units. Accordingly, a load-adaptive scheme is proposed in this paper by changing the dc-link output voltage dynamically, which in return can always ensure that the currents drawn by the rectifiers are equal, and thus a good quality of the total grid current is maintained. Experiments have verified the effectiveness of the proposal in terms of harmonic mitigation in a size- and cost-effective way for motor drive systems.

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